APPLICATION NOTE AN1707

TD220/221
Gate Driver with Vreg and Two-Point Regulator

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1 INTRODUCTION

This application note gives a simple functional description of the TD220/221, which is a standard circuit designed with an industrial application in mind, see *Figure 1*.

However, the TD220/221, together with other ST components, such as an ST7 microcontroller, and a MOSFET device, can provide a flexible, high-performance, power management solution that may be broadly applied to applications in the industrial fields.

A common problem in such off-line applications is the generation of a low voltage power supply for the various control ICs.

Because of this, the TD220/221 includes a "Two-Point Regulator" that enables control of a switching charge pump connected.

The charge pump diodes are integrated within the TD220/221, and a switch disables the charge pump when the nominal voltage is reached.

The main advantage of the TD220/221 is that it integrates, in a single SO8 package, 3 block functions—voltage regulation, power supply and power MOS driver—at a very reasonable price.

In typical applications, the TD220/221 manages the following functions:

- The MOSFET gate driver.
- The microcontroller's 3.3 V or 5 V supply.
- The power supply voltage at 13 V.

Fig. 1: Typical application schematic of the TD220/22

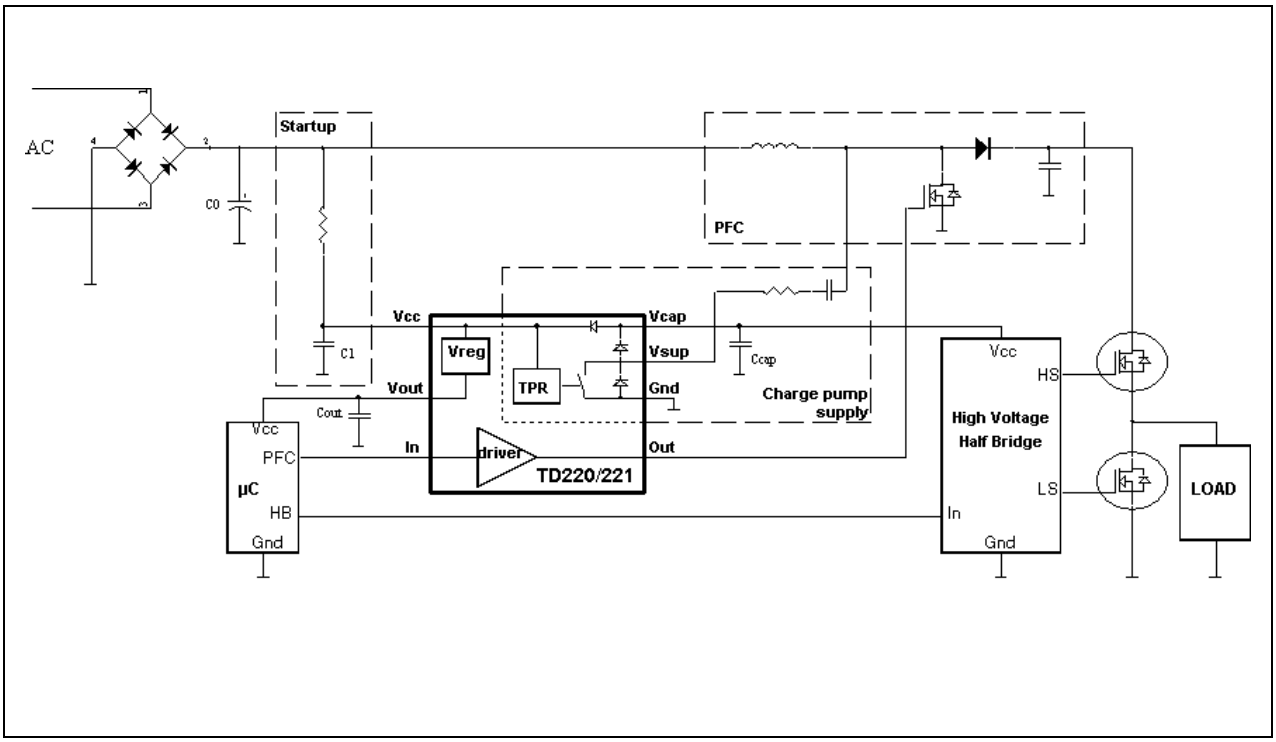


Fig. 2: Description of the TD220/221

As shown in *Figure 1*, the TD220/221 internal blocks are:

- Source—Used in order to bias other blocks in the circuit,
- UVLO—Under Voltage Lock Out,
- Vreg—Voltage Regulator at 3.3 V (for the TD220) or at 5 V (for the TD221),
- Driver—Provides the current in order to drive an external MOS,
- TPR—Two Point Regulator,
- Clamp—Fixes the maximum Vcc at 22 V.

The UVLO block insures that Vcc is set such that the TD220/221 functions correctly. Two boundary voltages are internally fixed at 14.1 V (UVLOH) and at 8.2 V (UVLOL). If the circuit is in the OFF state, it will turn on when the UVLO voltage reaches 14.1 V. This represents the minimum value necessary to turn the circuit ON, and then the Vcc power supply value stabilizes at 13 V. When the circuit is in the ON state, maximum UVLO voltage value that turns the circuit OFF is 8.2 V.

The role of the UVLO is both simple and extremely important: it imposes the voltage range for circuit ignition and blocking.

When the Vcc is at 13 V the Vreg block provides a precise output voltage at 3.3 V (for the TD220) or at 5 V (for the TD221) with accuracy of ±3% at 25°C and for Iout = 10 mA. This Vcc is used to supply power to the driver of an external power MOS.

The Vcc voltage is so exact thanks to the TPR block that allows it to maintain an accuracy of ±300 mV. This variation is measured using the external capacitor C1 = 100 nF as shown in *Figure 3* and *Figure 4*.

Fig. 3: TPR schematic: LDMOS Off

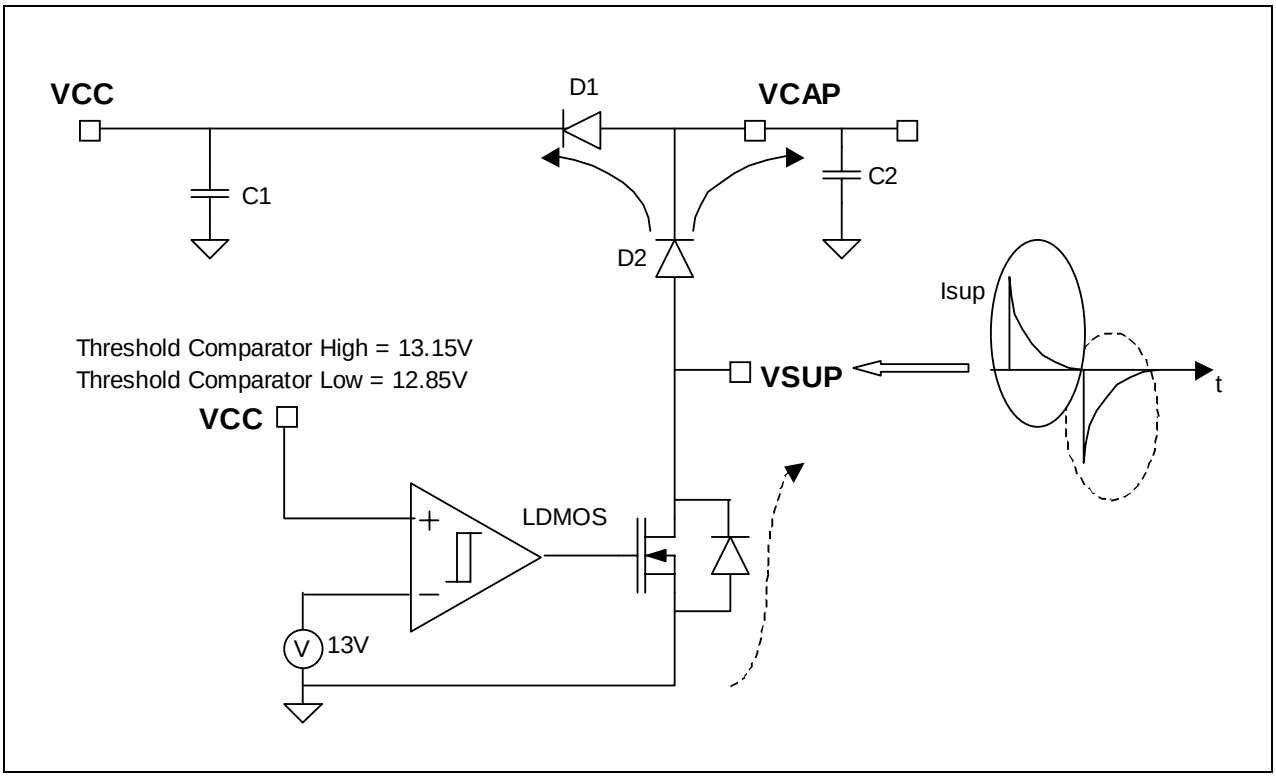
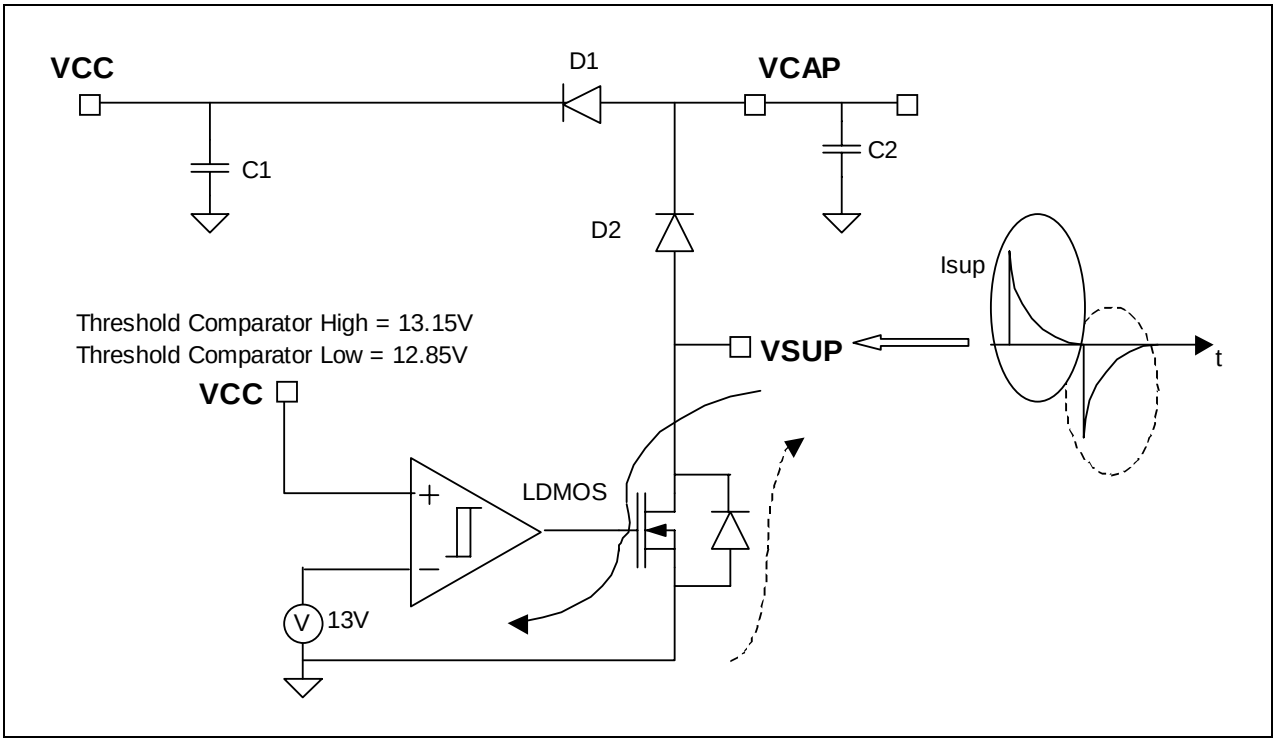


Fig. 4: TPR schematic: LDMOS On



The Vcc voltage is regulated by the power LDMOS, driven by the CMOS comparator with hysteresis.

When the LDMOS is in the OFF state, the energy arrives at the VSUP pin, and the current passes across the D1 and D2 diodes, charging the C1 and C2 capacitors, and increasing the Vcc voltage value.

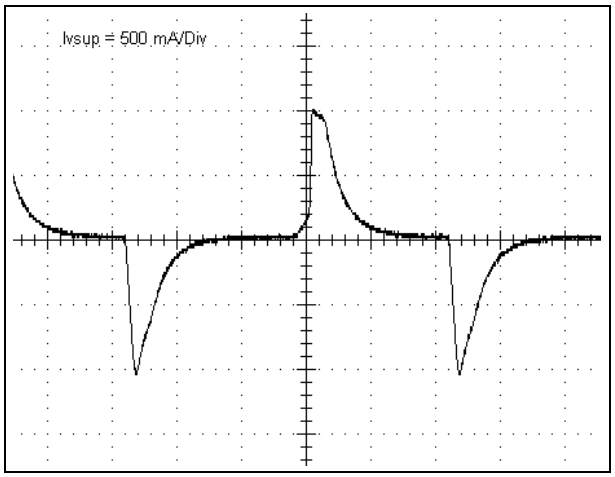
When the LDMOS is in the ON state, the energy discharges versus the ground and the Vcc voltage value decreases with reference to the application consumption.

As shown in *Figure 5*, it is possible to see the current behavior on the VSUP pin. This behavior is generated by an RC circuit supplied periodically with a duty cycle of 50%.

When the LDMOS is in the OFF state, the positive current pulse charges C1 and C2 capacitors and the negative current pulse goes across the internal LDMOS diode.

When the TPR threshold reaches Vtpron, almost 13.15 V, the comparator switches the LDMOS to the ON state.

Fig. 5: VSUP current behavior



In this case, the positive current pulse goes across the LDMOS (Ron) and discharges to ground, while the negative current pulse is divided between the Ron and the internal diode.

When Vcc voltage reaches Vtproff, almost 12.85 V, the comparator turns off the LDMOS and the current pulses charge the C1 and C2 capacitors again.

Figure 6 shows the above described behavior for the TD220/221 application.

2 UVLO START UP

The UVLO startup feature requires an off-line voltage, together with a resistor, to be connected to the Vcc pin, as shown in *Figure 1* on page 1.

The Vcc waveform at startup is shown in *Figure 7*. You should study the charging and discharging time of the C1 capacitor time in order to choose the optimum value of C1 for your application. The C1 value should insure a sufficient discharge delay time to avoid reaching the UVLOL voltage value (8.2 V) which would turn off the circuit before the first current pulses arrive.

Fig. 6: VSUP and VCAP dynamic behavior

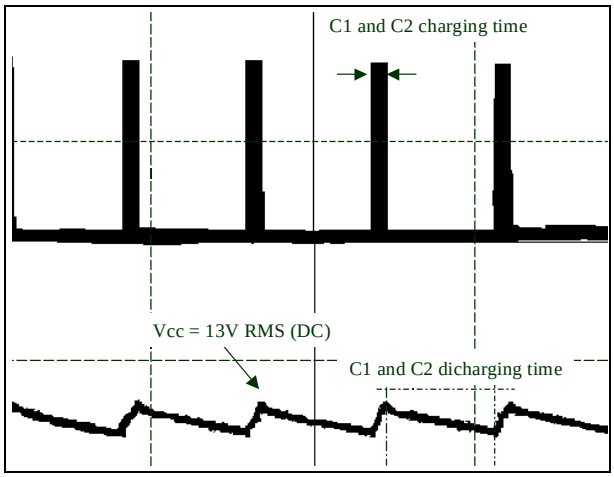
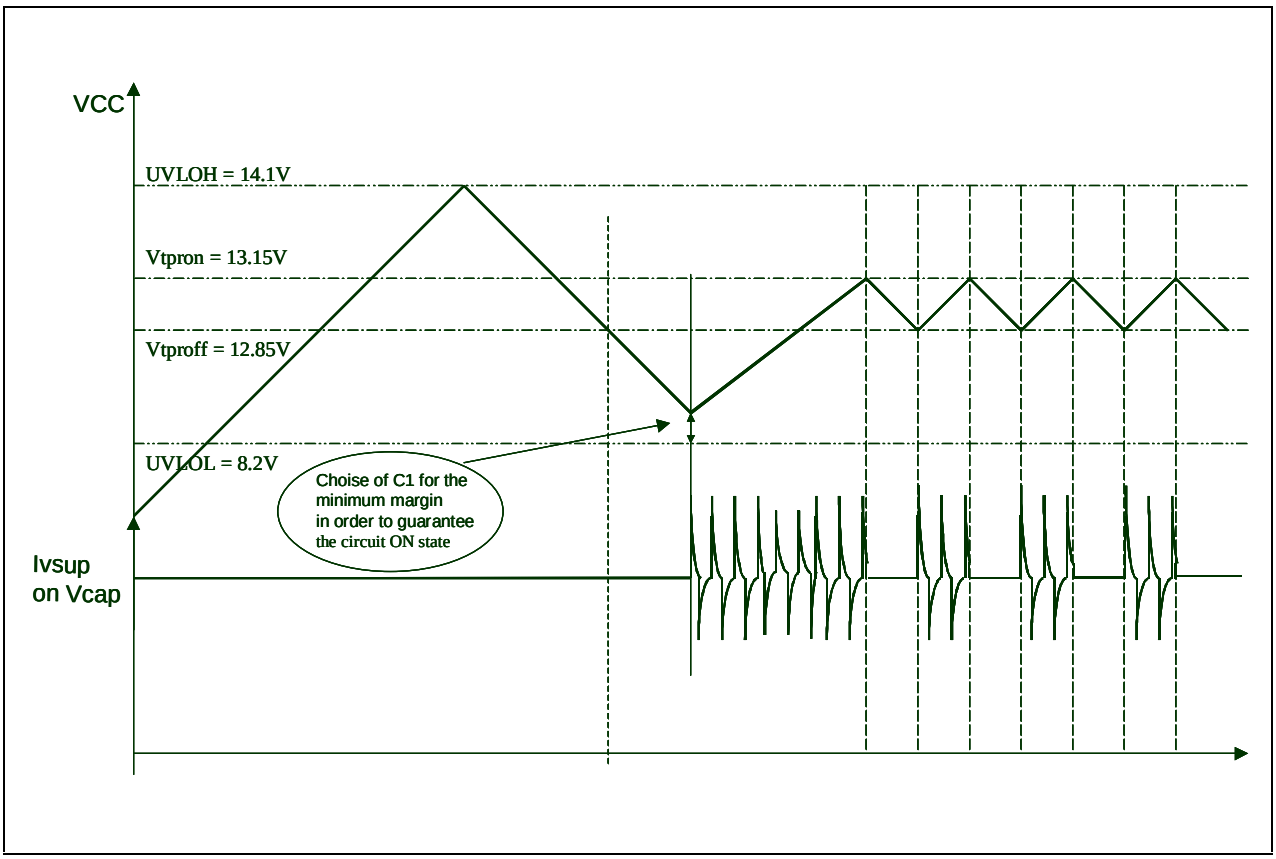


Fig. 7: UVLO Start Up and Ivsup


VCC
UVLOH = 14.1V
Vtpron = 13.15V
Vtproff = 12.85V
UVLOL = 8.2V
Choise of C1 for the minimum margin in order to guarantee the circuit ON state
Ivsup on Vcap

3 CONCLUSION

The TD220/221 has been designed for power managment applications in the industrial fields. This component integrates a Gate Driver with Vreg and Two-Point regulator in an SO8 plastic package. Good performance, excellent accuracy and low cost characterize this product.

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